

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A pull-up transistor array for a high voltage output circuit comprising:

a semiconductor substrate;

an epitaxial layer disposed on the semiconductor substrate;

N double diffused MOS transistors (DMOS transistor) laterally arranged in the epitaxial layer, each DMOS transistor having a source and a drain, wherein one of the source and drain surrounds the other of the source and drain, wherein one of a the source or drain of each double diffused MOS transistor is formed unique to each transistor, and wherein the N DMOS transistors share in common the other of the source or drain;

at least one ~~common~~ electrode for the one of the source or drain commonly shared among the N DMOS transistors; and

at least one unique electrode for the one of the source or drain of each of the double diffused MOS transistors that is formed unique to each of the DMOS transistors.

2. (Original) The pull-up transistor array for the high voltage output circuit as claimed in claim 1, wherein the DMOS transistor is an N-type vertical double diffused MOS transistor (nVDMOS transistor).

3. (Original) The pull-up transistor array for the high voltage output circuit as claimed in claim 1, wherein the DMOS transistor is a P-type lateral double diffused MOS transistor (pLDMOS transistor).

4. (Original) A pull-up transistor array for a high voltage output circuit comprising:

- a substrate of a first conductivity type;
- an epitaxial layer of a second conductivity type disposed on the substrate;
- a buried layer of the second conductivity type interposed between the substrate and the epitaxial layer;
- a plurality of looped insulating patterns regularly spaced and disposed on the epitaxial layer along one direction;
- a gate pattern disposed on an upper part of a region surrounded by the looped insulating pattern such that the gate pattern partially overlaps an upper portion of the looped insulating layer, and having a mesh-shaped structure in which with a plurality of openings are arranged two-dimensionally exposing the epitaxial layer;
- a drain region aligned to outer walls of the looped insulating patterns to be disposed vertically in the epitaxial layer between the looped insulating patterns; and
- a plurality of source regions disposed respectively in the epitaxial layer exposed through the openings of the gate patterns.

5. (Original) The pull-up transistor array as claimed in claim 4, wherein the drain region comprises:

- a drift layer of the second conductivity type vertically connected to the buried layer of the second conductivity type; and
- a heavily doped drain layer of the second conductivity type disposed in the drift layer of the second conductivity type.

6. (Original) The pull-up transistor array as claimed in claim 4, wherein each source region comprises:

a body region of the first conductivity type disposed in the epitaxial layer of each opening;

a heavily doped source layer of the second conductivity type disposed in an upper portion of the epitaxial layer in the body region of the first conductivity type; and

a pickup region of the first conductivity type disposed adjacent to the heavily doped source layer disposed in an upper portion of the epitaxial layer of the body region,

wherein the body region is laterally diffused from the heavily doped source layer of the second conductivity type by a fixed distance.

7. (Original) The pull-up transistor array as claimed in claim 4, further comprising source electrodes disposed on the gate pattern to output a high voltage, wherein each source electrode is connected in common to the source regions formed in the openings of the gate pattern.

8. (Original) The pull-up transistor array as claimed in claim 4, further comprising a plurality of drain electrodes connected to the drain region, wherein the high voltage is supplied to the drain electrodes.

9. (Original) The pull-up transistor array as claimed in claim 4, further comprising gate electrodes connected to the gate patterns to input a pull-up signal, respectively.

10. (Original) A pull-up transistor array for a high voltage output circuit, comprising:

a substrate of a first conductivity type;

an epitaxial layer of a second conductivity type disposed on the substrate;
a plurality of the first conductivity type wells regularly spaced and disposed in the epitaxial layer along one direction;
a second conductivity type well of a ladder shaped structure aligned to sidewalls of the first conductivity type wells, disposed in the epitaxial layer surrounding the first conductivity type wells;
looped gate patterns respectively disposed on the epitaxial layer, wherein the looped gate patterns overlap an upper portion of sidewalls of the first conductivity type well;
a looped insulating pattern interposed between the epitaxial layer and the looped gate patterns;
a source region aligned to outer walls of the looped insulating patterns, disposed in the second conductivity type well; and
a plurality of drain regions aligned to inner walls of the looped insulating patterns, respectively disposed in the first conductivity type well.

11. (Original) The pull-up transistor array as claimed in claim 10, wherein the source region comprises:

a heavily doped diffusion layer of the first conductivity type formed in an upper portion of the epitaxial layer in the second conductivity type well; and
a pickup region of the second conductivity type,
wherein the source layer of the first conductivity type surrounds the pickup region of the second conductivity type.

12. (Original) The pull-up transistor array for the high voltage output circuit as claimed in claim 10, wherein each drain region comprises:

a body region of the first conductivity type aligned to an inner wall of a corresponding looped insulating pattern to be formed in the first conductivity type well; and

a heavily doped drain layer of the first conductivity type formed in an upper portion of the epitaxial layer in the body region of the first conductivity type.

13. (Original) The pull-up transistor array as claimed in claim 10, further comprising drain electrodes connected to the drain regions to output a high voltage, respectively.

14. (Original) The pull-up transistor array as claimed in claim 10, further comprising a plurality of source electrodes connected to the source, region into which the high voltage is applied.

15. (Original) The pull-up transistor array for the high voltage output circuit as claimed in claim 10, further comprising a plurality of gate electrodes respectively connected to the gate pattern to input individually a plurality of pull-up signals.

16. (Previously Presented) The pull-up transistor array of claim 1, wherein the one of the source or drain commonly shared among the N DMOS transistors surrounds the one of the source or drain of each double diffused MOS transistor formed unique to each transistor.

17. (Previously Presented) The pull-up transistor array of claim 1, where the common electrode and unique electrodes are all disposed on a same side of the semiconductor substrate as each other.

18. (Previously Presented) The pull-up transistor array of claim 1, where the epitaxial layer is of a first conductivity type and the source and drain are of a second conductivity type different from the first conductivity type.

19. (Previously Presented) The pull-up transistor array of claim 1, where the epitaxial layer is of a first conductivity type, the source and drain are of the first conductivity type, and the substrate is of a second conductivity type different from the first conductivity type.

20. (Previously Presented) The pull-up transistor array of claim 1, further comprising a buried layer interposed between the substrate and the epitaxial layer, where the epitaxial layer and the buried layer each have a first conductivity type, and where the buried layer is more heavily doped than the epitaxial layer.

21. (Previously Presented) The pull-up transistor array of claim 1, where $N > 2$.